What is claimed is:

1. A semiconductor memory device having a plurality of memory banks sharing an address bus and a data bus, to which memory accessing is performed to a selected memory cell of a memory bank selected by an address,

each of said memory banks comprising:

an address register for holding a write address;

a data register for holding write data;

an address matching detection circuit for comparing an address held by said address register and an address input via said address bus and outputting an address matching signal when the two are matched; and

a control circuit for outputting write data held in said data register as read data from a memory cell specified by said read address when receiving said address matching signal indicating that write address held in said address register matches with read address to be input by said matching detection circuit when performing reading continuously from writing.

2. A semiconductor memory device as set forth in claim 1, comprising an address selection circuit for selecting either one of a write address held in said

address register and an address input from said address bus and outputting the selected address to a row decoder and a column decoder.

3. A semiconductor memory device as set forth in claim 1, comprising a data detection circuit for detecting whether data is held in said data register or not.

4. A semiconductor memory device as set forth in claim 3, further comprising a data transfer gate for outputting data held in said data register to a sense amplifier corresponding to a memory cell specified by said read address in accordance with a control signal from said control circuit when said data detection circuit detects that data is held in said data register.

5. A semiconductor memory device as set forth in claim 1, comprising a write gate for transferring write data input from a write data line to said data register in accordance with a write control signal to said data register when writing.

6. A semiconductor memory device as set forth in claim 1, wherein twist bit lines are used in a memory cell array in said memory bank.